

A Power Electronic Transformer-based Three-Phase PWM AC Drive with Lossless Commutation of Leakage Energy

Kaushik Basu, Apurva Somani, Krushna K Mohapatra, Member, *IEEE* and Ned Mohan Fellow, *IEEE*
 Department of Electrical and Computer Engineering
 University of Minnesota
 Minneapolis, Minnesota 55455
 Email: basux017@umn.edu

Abstract—This paper proposes a novel dc/ac converter topology with a high frequency ac-link for three-phase adjustable speed PWM ac drives. Such drives find applications in UPS systems and renewable energy sources like solar and fuel cells. This topology provides single-stage power conversion with bidirectional power flow capability. The high frequency transformer offers the benefits of galvanic isolation and high power density. The topology proposed in this paper minimizes the number of switching transitions between the transformer winding and the load. This reduces common-mode voltage switching and improves the output voltage profile. A lossless source based commutation technique has been developed for the commutation of the energy stored in the leakage inductances of the high frequency transformer. This method also results in zero current switching (ZCS) of all four-quadrant switches in the load side converter. The proposed topology has been analyzed and simulated. Simulation results that verify the operation of the proposed topology are presented.

I. INTRODUCTION

An inverter with high frequency ac-link finds applications in standby power supplies like UPS systems along with renewable energy sources like photovoltaic and fuel cells [1] [2]. The high frequency transformer provides necessary galvanic isolation and high power density by reducing the size of the magnetics. A conventional system involves a three-stage power conversion (dc-high frequency ac-dc-adjustable ac) and requires an electrolytic capacitor that reduces the reliability of the system. A more direct power conversion is possible. Such systems can generally be classified as either resonant or non-resonant. Resonant converters contain reactive elements and their output voltage depends on loading [3] [4]. Non-resonant converters use the conventional PWM control of adjustable speed ac drives. They maintain a constant frequency of the ac-link and practically do not need any reactive elements.

Fig. 1 shows the schematic of a single-phase dc/ac inverter with high frequency ac-link [5] [6]. It is known that when the output current and voltage are in the same quadrant, this converter can be operated like a phase-shifted full-bridge converter in order to get soft switching in most of the switches [7].

The schematic of a three-phase dc/ac inverter with high frequency ac-link is shown in Fig. 2. This topology

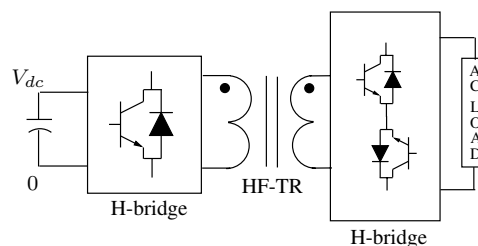


Fig. 1. Single-phase dc/ac inverter with high frequency ac-link

was first proposed in [6]. Here the H-bridge in the input of the converter converts the input dc voltage to a high frequency square wave ac voltage. The output cycloconverter converts the high frequency ac voltage to a variable magnitude and frequency PWM output voltage. In [8], it has been identified that since the three-phase load is of inductive nature, every time the output cycloconverter changes its switching state, the energy stored in the leakage inductances of the transformer needs to be commutated. A source-based lossless commutation of the leakage energy is proposed in [8]. In [3], an auxiliary circuit and control method has been suggested in order to get soft switching. In [2], a carrier based PWM technique has been suggested for the output cycloconverter.

Transition of each switching state of the output cycloconverter requires commutation of leakage energy and that results in loss in output voltage [3], distortion in the output current and common-mode voltage switching. Also the commutation process requires a sequence of complicated switching at variable instants of time. If the

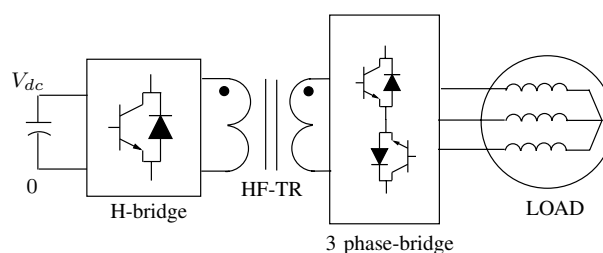


Fig. 2. Three-phase dc/ac inverter with high frequency ac-link

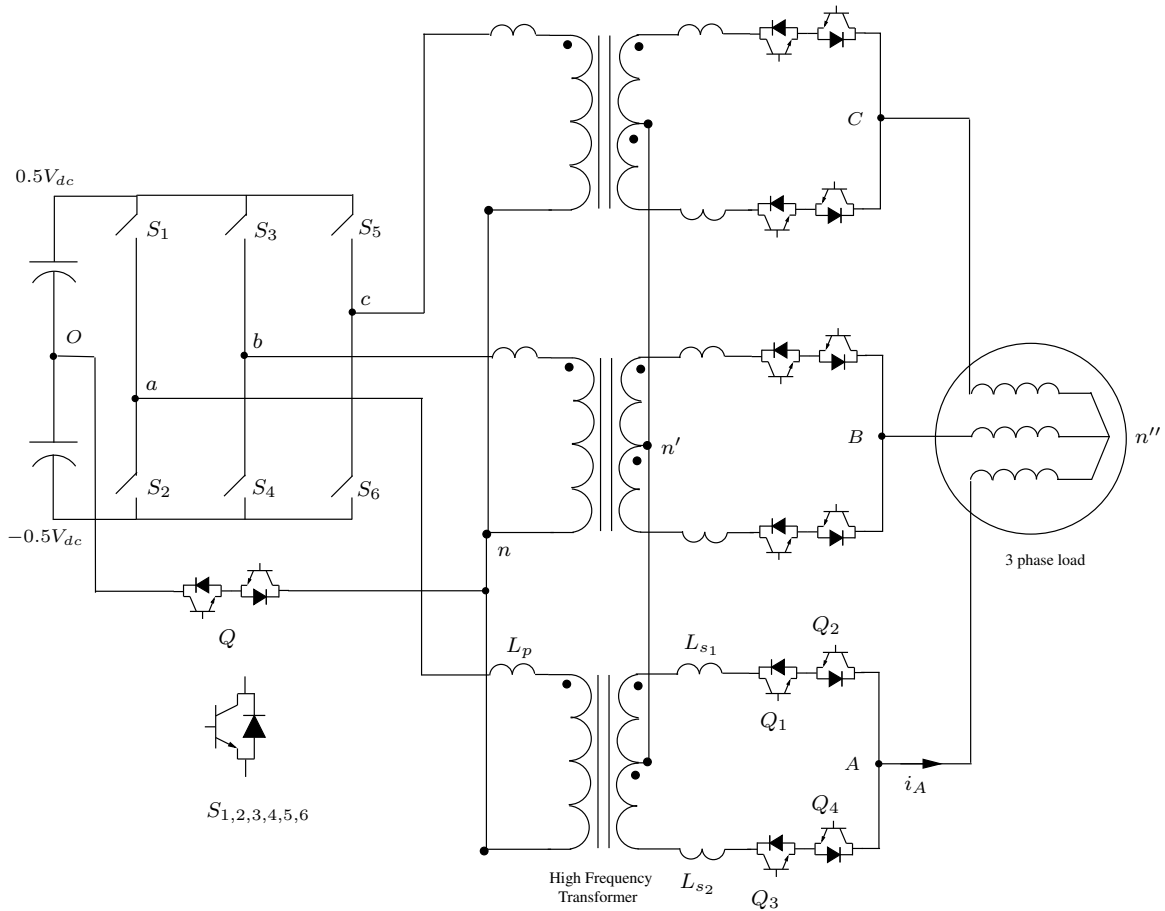


Fig. 3. Circuit diagram of the proposed topology

output cycloconverter is operated with conventional space vector PWM (CSVPWM), it changes its state six times in a subcycle over which the average output voltage vector is synthesized.

This paper proposes an alternative topology (Fig. 3) where the PWM voltage is synthesized in the input two level converter and output consists of three square wave modulated cycloconverters. This topology minimizes the switching transitions between the transformer leakage inductance and the output inductive load. Leakage energy needs to be commutated only once in a subcycle. This paper also presents a lossless commutation strategy of the leakage energy. This idea of commutation can be applied to the single-phase topology given in Fig. 1. All the switches in the output cycloconverter are soft switched (ZCS).

II. ANALYSIS

A. PWM Strategy for the Front-End Inverter

The basic operation of this converter is divided into two parts: power transfer and commutation. Fig. 4 shows the different control signals that govern these two modes over one cycle of operation. The signal PT refers to power transfer mode. The complement of PT is CT and it refers to commutation. The following analysis refers to the output converter for phase-A. Over one cycle, the

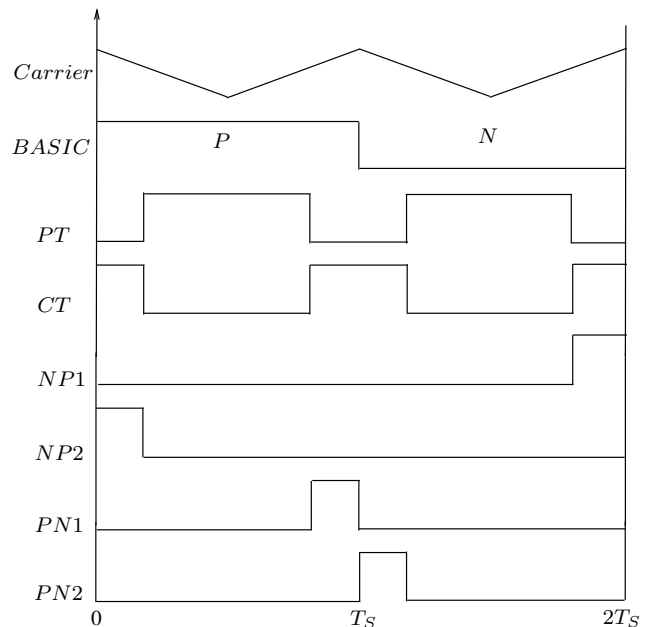


Fig. 4. Control signals

signal *BASIC* has two states: positive and negative. These states are denoted by *P* and *N* in Fig. 4. During the positive state, switches *Q1* and *Q2* are ON and power

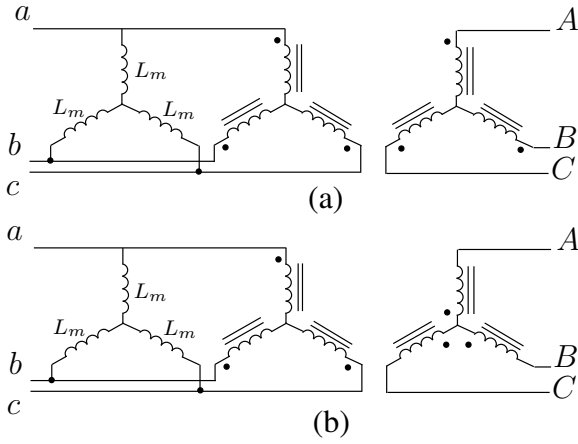


Fig. 5. Circuit configuration during a) positive b) negative states of power transfer

is transferred through the upper half of the secondary winding. During the negative state, switches Q_3 and Q_4 are ON and power is transferred through the lower half of the secondary winding. The star point of the primary windings (n) and the mid-point (O) of the input dc bus is connected with a four quadrant switch Q , (Fig. 3). During the power transfer mode the switch Q is turned OFF in order to prevent the flow of common-mode current.

In this topology, the output three-phase load appears to be in parallel with the star-connected magnetizing inductances seen from the primary side as shown in Fig. 5. During the positive half of the power transfer interval, the required output voltage vector is generated on an average by switching the input inverter. During the other half, negative of the required output voltage vector is generated by the input inverter. The output cycloconverter inverts this voltage vector and applies the correct voltage vector to the load. The net average voltage vector applied to the magnetizing inductances is zero. So the required flux balance in the transformer is achieved over one cycle of operation for the power transfer mode.

The PWM signals for the input inverter during power transfer mode are generated using the triangle comparison method. This is the carrier based method of generation of conventional space vector PWM (CSVPWM). The duty ratios of the switches S_1 , S_3 and S_5 are given by (1). The duty ratios given by (1) are derived using (2), (3) and (4). These duty ratio signals are compared with a triangular carrier in order to generate PWM signals for the input inverter during the power transfer mode (Fig. 6). The switches in each leg of the inverter are switched in a complementary fashion.

The input dc bus voltage is V_{dc} . N_p and N_s respectively denote the number of turns in the primary and each half of the secondary windings of the transformer. In (2) m denotes modulation index and it is defined such that the peak of the generated average line to neutral voltage at the output is $mV_{dc} \left(\frac{N_s}{N_p} \right)$. The maximum value of m

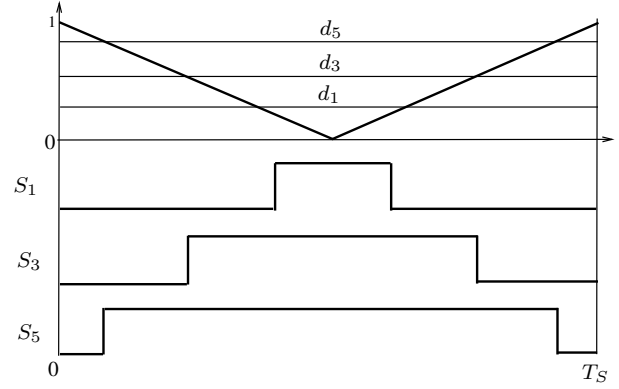


Fig. 6. Front end inverter PWM generation

is $\frac{1}{\sqrt{3}}$. The frequency of the synthesized output voltage waveform is ω .

$$\begin{aligned} d_1(t) &= m(t) \cos \omega t + d_{cm}(t) \\ d_3(t) &= m(t) \cos \left(\omega t - \frac{2\pi}{3} \right) + d_{cm}(t) \\ d_5(t) &= m(t) \cos \left(\omega t + \frac{2\pi}{3} \right) + d_{cm}(t) \end{aligned} \quad (1)$$

$$m(t) = \begin{cases} +m & \text{first half of power transfer} \\ -m & \text{next half of power transfer} \end{cases} \quad (2)$$

$$d_{cm}(t) = \frac{1}{2} + \frac{x(t)}{2} \quad (3)$$

$$x(t) = \text{mid} \left[\begin{aligned} &m(t) \cos \omega t, \\ &m(t) \cos \left(\omega t - \frac{2\pi}{3} \right), \\ &m(t) \cos \left(\omega t + \frac{2\pi}{3} \right) \end{aligned} \right] \quad (4)$$

B. Commutation

During commutation, the current in the primary winding changes direction. Also, in the secondary windings, the current transfers from one half to the other half. The process of commutation occurs whenever the power transfer mode changes from one state to the other (positive-to-negative or negative-to-positive). The transformer windings have leakage inductances which are shown in Fig. 3. L_p is the leakage inductance of the primary winding. L_{s1} and L_{s2} are the leakage inductances present in the upper and lower half of the secondary winding respectively.

In order to change the current through these leakage inductances, appropriate voltages need to be applied. In this topology, these voltages are applied by the input converter. Since the input converter uses the input dc voltage, there is no energy loss associated with the commutation process. Depending on the direction of the output current and type

of the change in the power transfer mode (positive-to-negative or otherwise), the commutation process can be classified into four different cases.

Here, details of one of the four cases of commutation in one phase (phase-A) are presented. The commutation mechanism is same for all the three phases. In the case described here,

- 1) the power transfer mode is changing from negative to positive
- 2) the load current is negative ($i_A < 0$)

Tables I and II describe the details of the commutation process for all four cases. Fig. 7 shows the circuit configurations during the commutation process. Since the commutation period is much smaller with respect to the time period of the output load current, the load can be modeled as a dc current source during the commutation process.

Fig. 7(a) shows the power transfer through the lower

TABLE I
 $i_{out} > 0$

	Q_1	Q_2	Q_3	Q_4	S_1	Q	D_1	D_2	D_3	D_4
P	1	1	0	0	X	0	0	1	0	0
PN1a	1	0	0	0	0	1	0	1	0	0
PN1b	1	0	1	0	0	1	0	1	0	1
PN2	0	0	1	1	1	1	0	0	0	1
N	0	0	1	1	X	0	0	0	0	1
NP1a	0	0	1	0	1	1	0	0	0	1
NP1b	1	0	1	0	1	1	0	1	0	1
NP2	1	1	0	0	0	1	0	1	0	0

TABLE II
 $i_{out} < 0$

	Q_1	Q_2	Q_3	Q_4	S_1	Q	D_1	D_2	D_3	D_4
P	1	1	0	0	X	0	1	0	0	0
PN1a	0	1	0	0	1	1	1	0	0	0
PN1b	0	1	0	1	1	1	1	0	1	0
PN2	0	0	1	1	0	1	0	0	1	0
N	0	0	1	1	X	0	0	0	1	0
NP1a	0	0	0	1	0	1	0	0	1	0
NP1b	0	1	0	1	0	1	1	0	1	0
NP2	1	1	0	0	1	1	1	0	0	0

half of the secondary winding, switch Q_4 and diode D_3 are conducting. Note that the switch Q is open during the power transfer mode. The commutation is done on a phase-by-phase basis. A proper voltage needs to be applied to the primary of each phase, independent of the other phases. This is the reason why the switch Q is turned ON during commutation. Commutation starts when PT goes low and CT goes high. NP1 is high during the first part of the commutation process and NP2 is high during the second stage (Fig. 4). The first stage of NP1 is referred as NP1a in the Tables I and II. In this stage switch Q_3 is turned OFF and Q is turned ON. In this commutation, a negative voltage needs to be applied to the transformer primary since $i_A < 0$. So the switch S_2 is turned ON. During the second stage of NP1 (referred to as NP1b), switch Q_2 is turned ON. This forward biases the diode D_1 and current i_{s1} starts building in the upper half of the primary winding (Fig. 7(b)). The equivalent

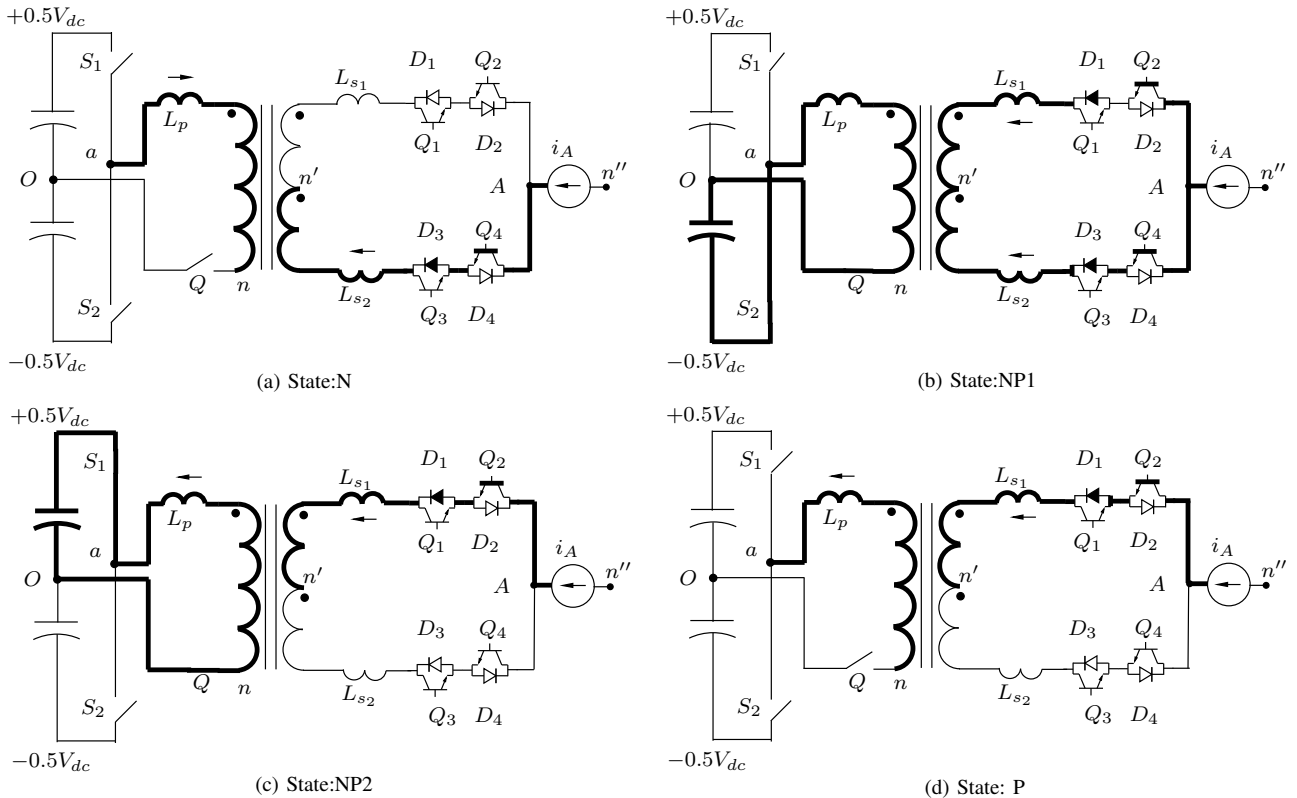


Fig. 7. Circuit configuration at four stages of commutation

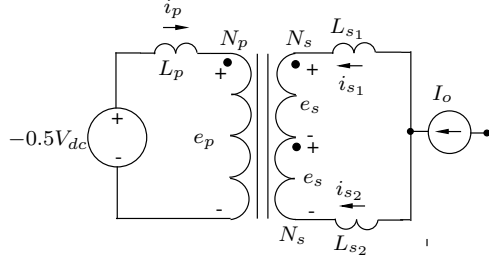


Fig. 8. The equivalent circuit during commutation

circuit of this stage is given by the Fig. 8. I_o is the value of i_A during this time.

In order to find the time required to finish the commutation process, the circuit in Fig. 8 needs to be analyzed. In this analysis, the magnetizing component of the transformer current is neglected. This assumption and Ampere's law results in (5). Faraday's law implies (6). Application of KCL at the load terminal gives (7). Applying KVL to the primary and secondary winding gives (8) and (9) respectively. The solution of these equations leads to (10). So the maximum time required to finish the commutation process (t_{com}) is given by (11) where i_{omax} is the peak of the sinusoidal output current. Setting t_{com} as the commutation time will ensure sufficient time for commutation at all other load conditions.

When current i_{s1} reaches the load current i_A , i_{s2} becomes zero. Because of the diode D_3 the current i_{s2} can not become negative and the commutation process ends automatically. The duration for the pulse NP1 must be slightly more than t_{com} . The turn-ON transition of Q and Q_2 happens with zero current switching (ZCS).

$$i_{s1}N_s + i_pN_p - i_{s2}N_s = 0 \quad (5)$$

$$\frac{e_p}{N_p} = \frac{e_s}{N_s} \quad (6)$$

$$I_o = i_{s1} + i_{s2} \quad (7)$$

$$0.5V_{dc} + e_p + L_p \frac{d}{dt} i_p = 0 \quad (8)$$

$$2e_s + L_{s1} \frac{d}{dt} i_{s1} - L_{s2} \frac{d}{dt} i_{s2} = 0 \quad (9)$$

$$\frac{d}{dt} i_{s1} = \frac{0.5V_{dc} \left(\frac{N_s}{N_p} \right)}{\left(\frac{L_{s1} + L_{s2}}{2} \right) + 2L_p \left(\frac{N_s}{N_p} \right)^2} \quad (10)$$

$$t_{com} = \left[\frac{\left(\frac{L_{s1} + L_{s2}}{2} \right) + 2L_p \left(\frac{N_s}{N_p} \right)^2}{0.5V_{dc} \left(\frac{N_s}{N_p} \right)} \right] i_{omax} \quad (11)$$

In the beginning of next stage (Fig. 7(c)), when NP2 goes high, switch Q_4 is turned off with ZCS. In order to maintain the true bidirectional nature of the converter, switch Q_1 is turned ON (to allow for possible change in

current direction in the upcoming power transfer mode). The switch $S1$ is turned ON in order to apply a positive voltage to the transformer primary. The duration of NP1 and NP2 are same. The Q switch current becomes zero at the end of NP2. Q is turned off at this instant with zero current (ZCS). The commutation process is now over and the converter goes into the positive state of the power transfer mode (Fig. 7(d)).

When CT is high, the switch Q is ON. The current through the switch Q has two components. One of them is the sum of the reflected currents flowing through the secondary. As the load is balanced this current is non zero only during the commutation stage. The other component is the sum of the magnetising currents of all three phases. At the beginning of the commutation stage when CT goes high this current is also zero. The net change in the sum of the magnetising currents during the commutation stage, when CT is high, is zero.

To show this let us consider a special case when load currents i_A and i_B are negative and i_C is positive and power transfer is changing from positive to negative half. As the load neutral point is not connected, (12) holds. This particular case implies (13). During the first half of the commutation when NP1 is high, voltages applied at the primary of A and B phases are $0.5V_{dc}$. $-0.5V_{dc}$ is applied to C phase. t_A , t_B and t_C are the times for actual commutation. Due to (11), t_A is proportional to the magnitude of the instantaneous current in phase A i.e. $|i_A|$. t_c is the duration of pulses NP1 and NP2 and is chosen such that it is more than maximum possible commutation time (t_{com}).

$$i_A + i_B + i_C = 0 \quad (12)$$

$$|i_C| = |i_A| + |i_B| \quad (13)$$

$$t_C = t_A + t_B \quad (14)$$

$$e_A = 0.5V_{dc} - L_p \frac{d}{dt} i_p \quad (15)$$

$$e_A = \left[1 - \frac{2}{\left(\frac{L_{s1} + L_{s2}}{2} \right) \left(\frac{N_p}{N_s} \right)^2 + 2L_p} \right] 0.5V_{dc} \quad (16)$$

$$e_A = e_B = -e_C \quad (17)$$

TABLE III
PARAMETERS

L_{load}	10mH
R_{load}	2.5Ω
L_p	50μH
R_p	0.2Ω
L_{s1}, L_{s2}	25μH
R_{s1}, R_{s2}	5mΩ
L_m	15mH

$$\begin{aligned}\Delta i_{mA} &= \frac{t_A e_A}{L_m} + \frac{(t_c - t_A)V_{dc}}{2L_m} - \frac{t_c V_{dc}}{2L_m} \\ &= \frac{t_A}{L_m} (e_A - 0.5V_{dc})\end{aligned}\quad (18)$$

e_A is the voltage that appears across the magnetizing inductance of the transformer in phase A. Due to KVL, e_A is given by (15). In this particular case this implies (16). Similarly it is possible to show that (17) holds. The change in the magnetizing current in phase A during this time, is given by (18). L_m is the magnetizing inductance. Similar expressions can be obtained for Δi_{mB} and Δi_{mC} . By (14) and (17) the net change in the sum of these three magnetizing currents during the time for which NP1 and NP2 are high is zero (19). The switch Q is turned OFF with zero current.

$$\Delta i_{mA} + \Delta i_{mB} + \Delta i_{mC} = 0 \quad (19)$$

C. Simulation results

The circuit in Fig. 3 is simulated in MATLAB/Simulink. The input dc bus voltage, V_{dc} , is set to 500 V. The output is connected to a balanced three-phase RL load. The load is star-connected. The parameters of the circuit are given in Table III. The modulation index m is set at 0.25. The frequency ($f_s = \frac{1}{T_s}$) at which the output voltage is synthesized on an average is 5 kHz. The effective frequency at which the transformer flux is balanced is 2.5 kHz. The commutation time t_{com} is calculated as $16.6 \mu s$ according to (11). The frequency of the output voltage is set to 45 Hz.

Fig. 9 shows the output load current and the current through the upper half of the winding in phase-A. It is clear from this figure that each half of the secondary winding conducts only for 50% of time. Fig. 10 describes the commutation process. The signal ON is the combination of signals NP1 and NP2. Similarly, OFF is the combination of PN1 and PN2. The current through the inductor L_{s1} changes linearly during the commutation according to the slope predicted by (10). Fig. 10 also shows the current through the switch Q and the sum of the magnetizing currents. The net change in the sum of the magnetizing currents, $i_{m,sum}$, during ON and OFF is zero as predicted. The current through the switch Q is also zero at the beginning and at the end of the commutation. Thus, the simulation results confirm the soft switching (ZCS) of all of the four-quadrant switches. Fig. 11 shows the magnetizing current for one of the transformers. This figure verifies the flux balance in the transformer core and its high frequency operation.

III. CONCLUSION

In this paper, a new converter topology with a high frequency ac-link for three-phase PWM drives has been proposed. The proposed topology has the following extra benefits when compared to conventional drives with high frequency ac-links:

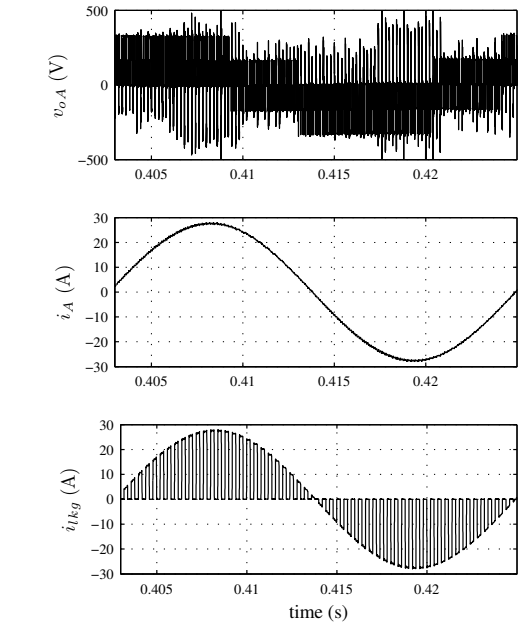


Fig. 9. Simulation results: Output voltage, output current, and current through upper half of secondary winding

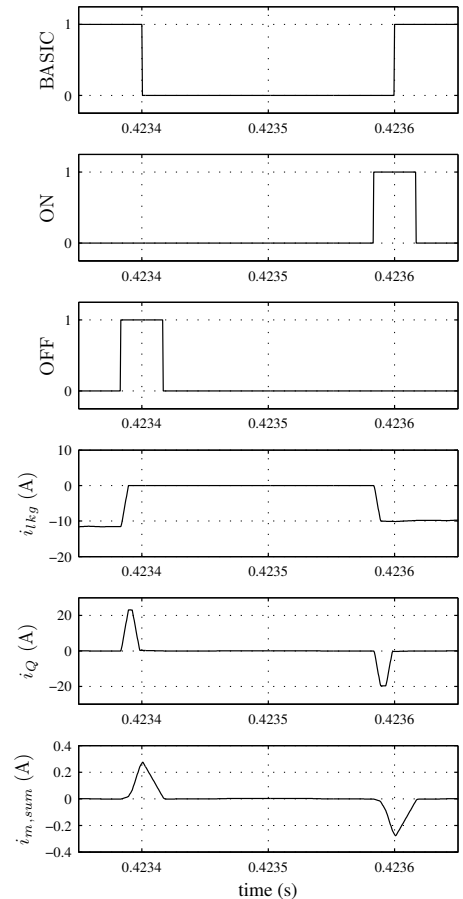


Fig. 10. Simulation results: Commutation process

- 1) Reduced common-mode voltage switching
- 2) Improved output voltage profile
- 3) Lossless commutation of leakage inductance energy

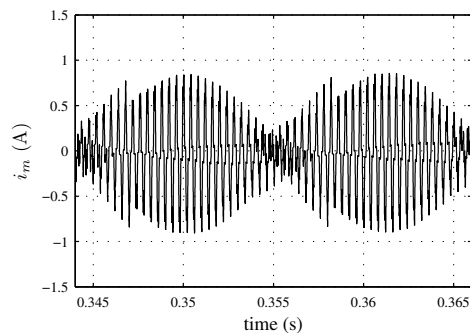


Fig. 11. Simulation results: Magnetizing current

4) Zero current switching (ZCS) for all bidirectional switches

The converter has been analyzed and strategies for output voltage generation and commutation have been described. Simulation has been performed with a non-ideal transformer by taking the leakage inductances into account. Simulation results have been presented which verify the converter's operation. The proposed topology offers a promising solution to the power electronic transformer problem. It can be modified and applied to a direct ac/ac conversion with high frequency ac-link problem as well.

REFERENCES

- [1] V. John, N. Mohan, E. Persson, and R. Nilssen, "High frequency isolation in standby power supplies which compensate load harmonic currents," in *Industrial Electronics, Control, and Instrumentation, 1993. Proceedings of the IECON '93., International Conference on*, Nov 1993, pp. 1264–1268 vol.2.
- [2] P. Krein, R. Balog, and X. Geng, "High-frequency link inverter for fuel cells based on multiple-carrier pwm," *Power Electronics, IEEE Transactions on*, vol. 19, no. 5, pp. 1279–1288, Sept. 2004.
- [3] B. Ozpineci and B. Bose, "Soft-switched performance-enhanced high frequency nonresonant link phase-controlled converter for ac motor drive," in *Industrial Electronics Society, 1998. IECON '98. Proceedings of the 24th Annual Conference of the IEEE*, vol. 2, Aug-4 Sep 1998, pp. 733–739 vol.2.
- [4] J. Gafford, M. Mazzola, J. Robbins, and G. Molen, "A multi-kilowatt high-frequency ac-link inverter for conversion of low-voltage dc to utility power voltages," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, June 2008, pp. 3707–3712.
- [5] S. Manias, P. Ziogas, and G. Oliver, "Bilateral dc to ac converter employing a high frequency link," in *Industry Applications Society Annual Meeting, 1985., Conference Record of the 1985 IEEE*, 1985, pp. 1156–1162.
- [6] T. Kawabata, K. Honjo, N. Sashida, K. Sanada, and M. Koyama, "High frequency link dc/ac converter with pwm cycloconverter," in *Industry Applications Society Annual Meeting, 1990., Conference Record of the 1990 IEEE*, Oct 1990, pp. 1119–1124 vol.2.
- [7] S. Deng, H. Mao, J. Mazumdar, I. Batarseh, and K. Islam, "A new control scheme for high-frequency link inverter design," in *Applied Power Electronics Conference and Exposition, 2003. APEC '03. Eighteenth Annual IEEE*, vol. 1, Feb. 2003, pp. 512–517 vol.1.
- [8] M. Matsui, M. Nagai, M. Mochizuki, and A. Nabae, "High-frequency link dc/ac converter with suppressed voltage clamp circuits-naturally commutated phase angle control with self turn-off devices," *Industry Applications, IEEE Transactions on*, vol. 32, no. 2, pp. 293–300, Mar/Apr 1996.